Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT REGISTER-BASED REFRESH ADDRESS GENERATION CIRCUIT
Inventor's Name: MORI et al
Application No.: New Application
Docket No.: 108273-00007

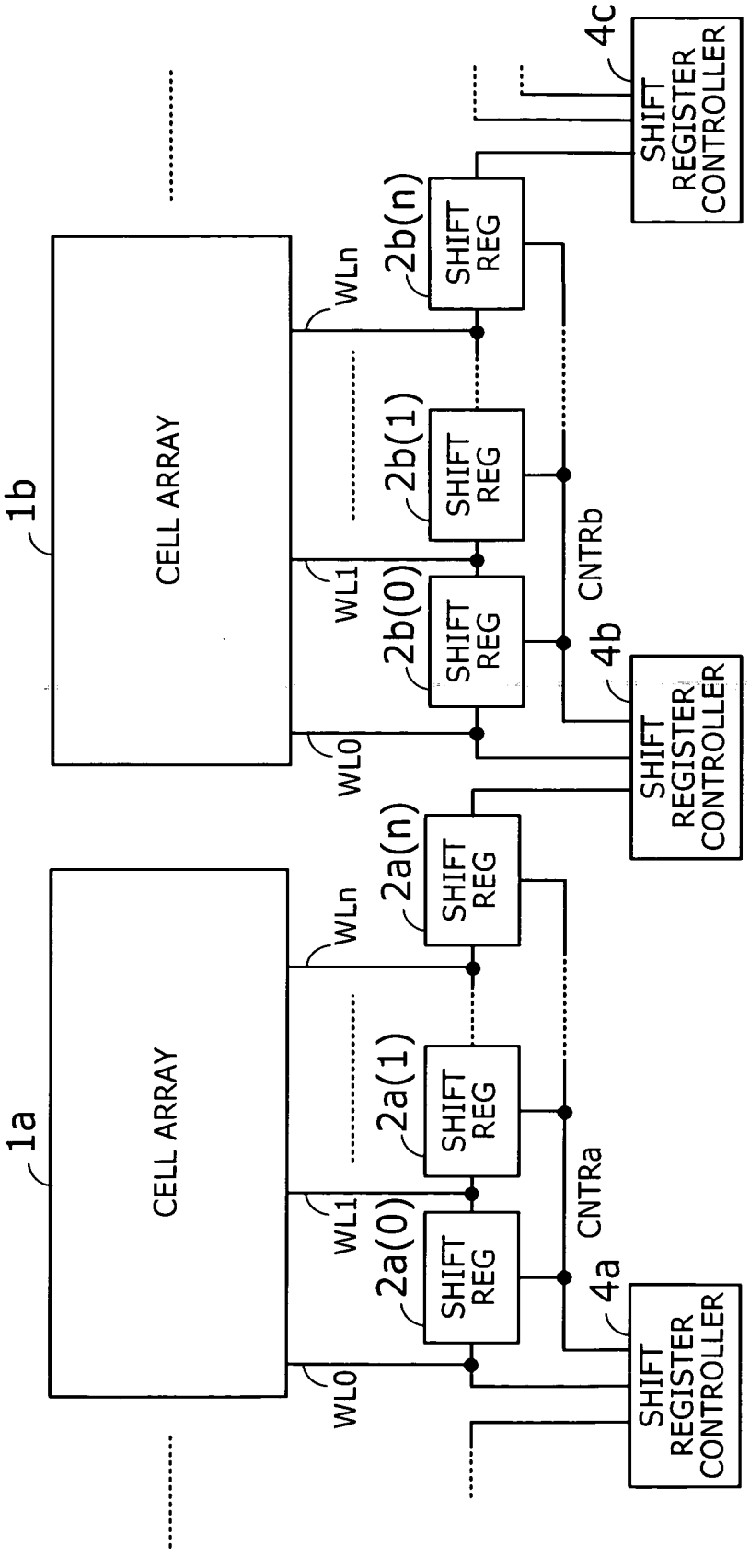
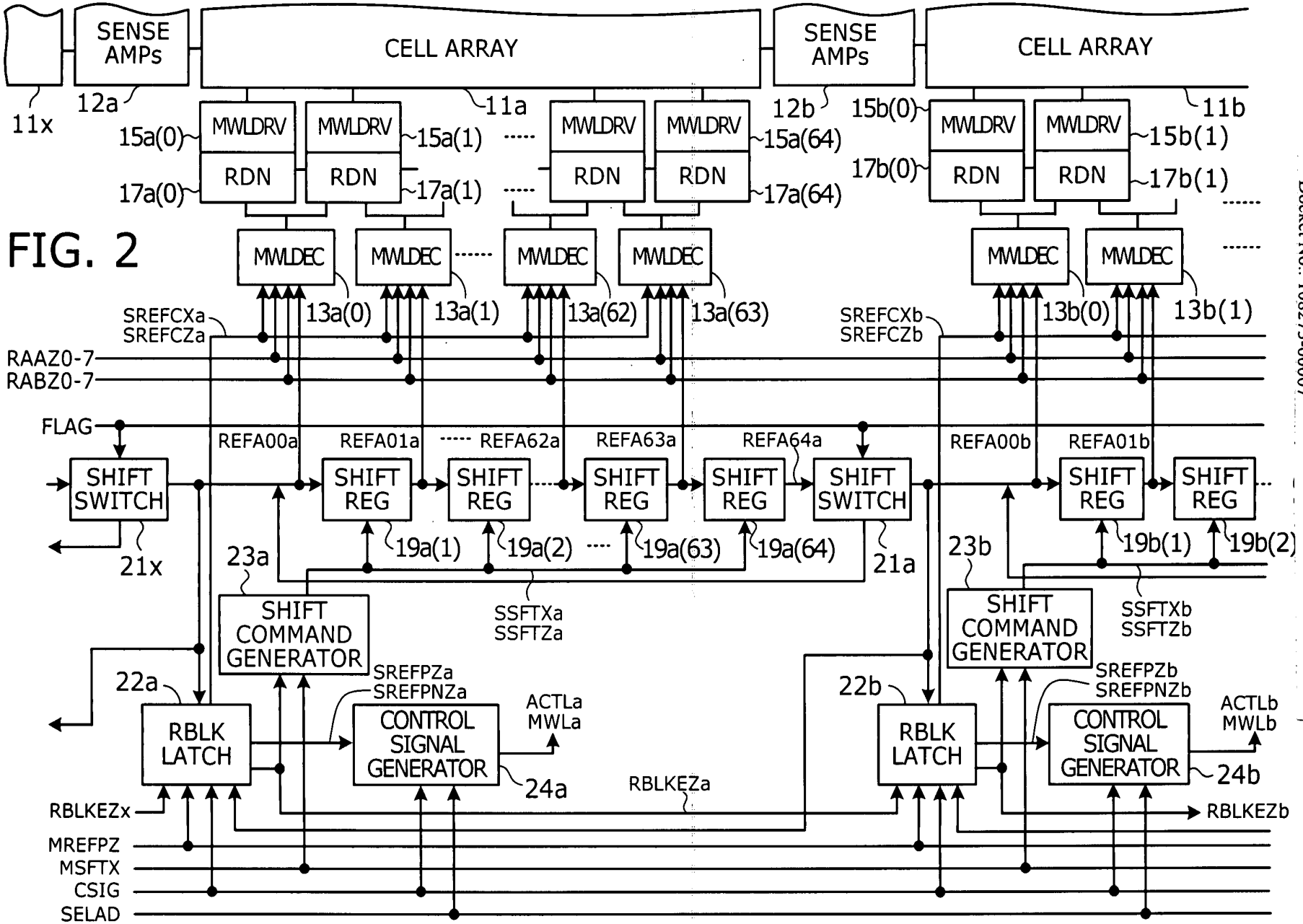


FIG. 1

FIG. 2


SENSE AMPs
CELL ARRAY
SENSE AMPs
CELL ARRAY
11x
12a
11a
12b
11b
15a(0)
15a(1)
15a(64)
15b(0)
15b(1)
17a(0)
17a(1)
17a(64)
17b(0)
17b(1)
MWLDRV
RDN
MWLDEC
13a(0)
13a(1)
13a(62)
13a(63)
13b(0)
13b(1)
SREFCXa
SREFCZa
SREFCXb
SREFCZb
RAAZ0-7
RABZ0-7
FLAG
REFA00a
REFA01a
REFA62a
REFA63a
REFA64a
REFA00b
REFA01b
SHIFT SWITCH
SHIFT REG
21x
21a
19a(1)
19a(2)
19a(63)
19a(64)
19b(1)
19b(2)
23a
23b
SHIFT COMMAND GENERATOR
SSFTXa
SSFTZa
SSFTXb
SSFTZb
22a
22b
RBLK LATCH
SREFPZa
SREFPNZa
SREFPZb
SREFPNZb
CONTROL SIGNAL GENERATOR
ACTLa
MWLa
ACTLb
MWLb
24a
24b
RBLKEZa
RBLKEZx
RBLKEZb
MREFPZ
MSFTX
CSIG
SELAD

13a(0) **WORD LINE DECODER**

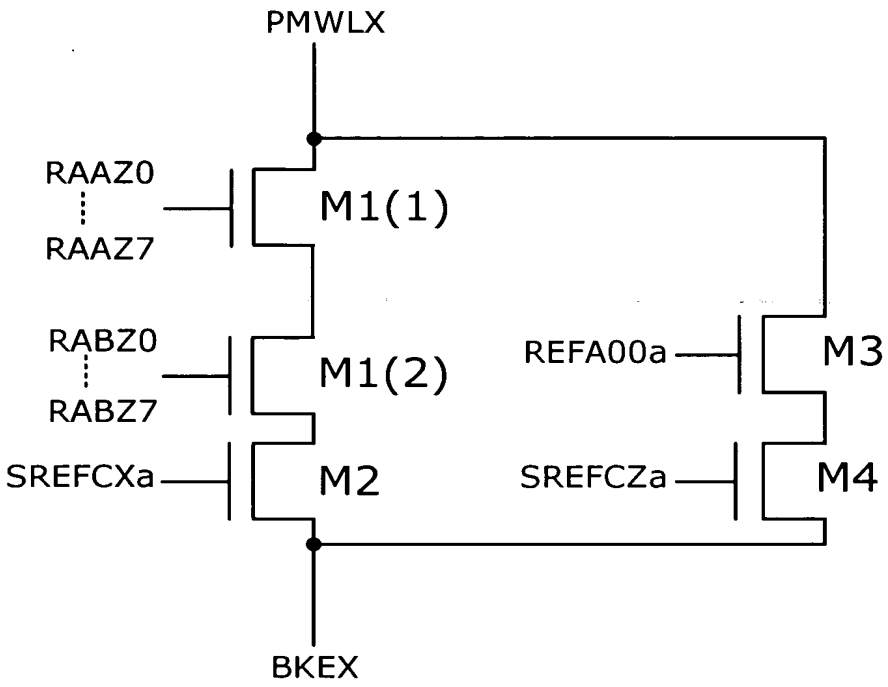


FIG. 3

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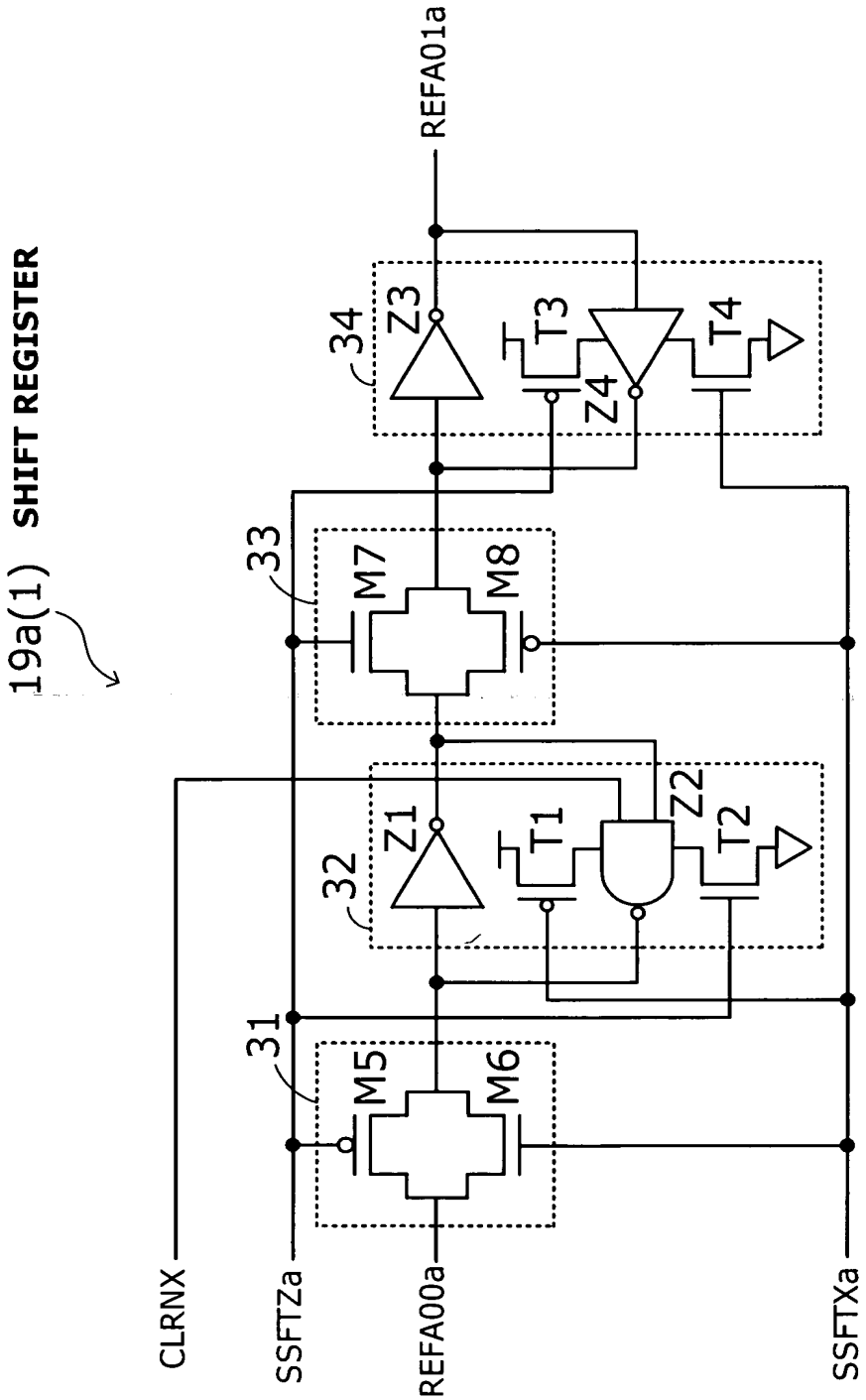

FIG. 4

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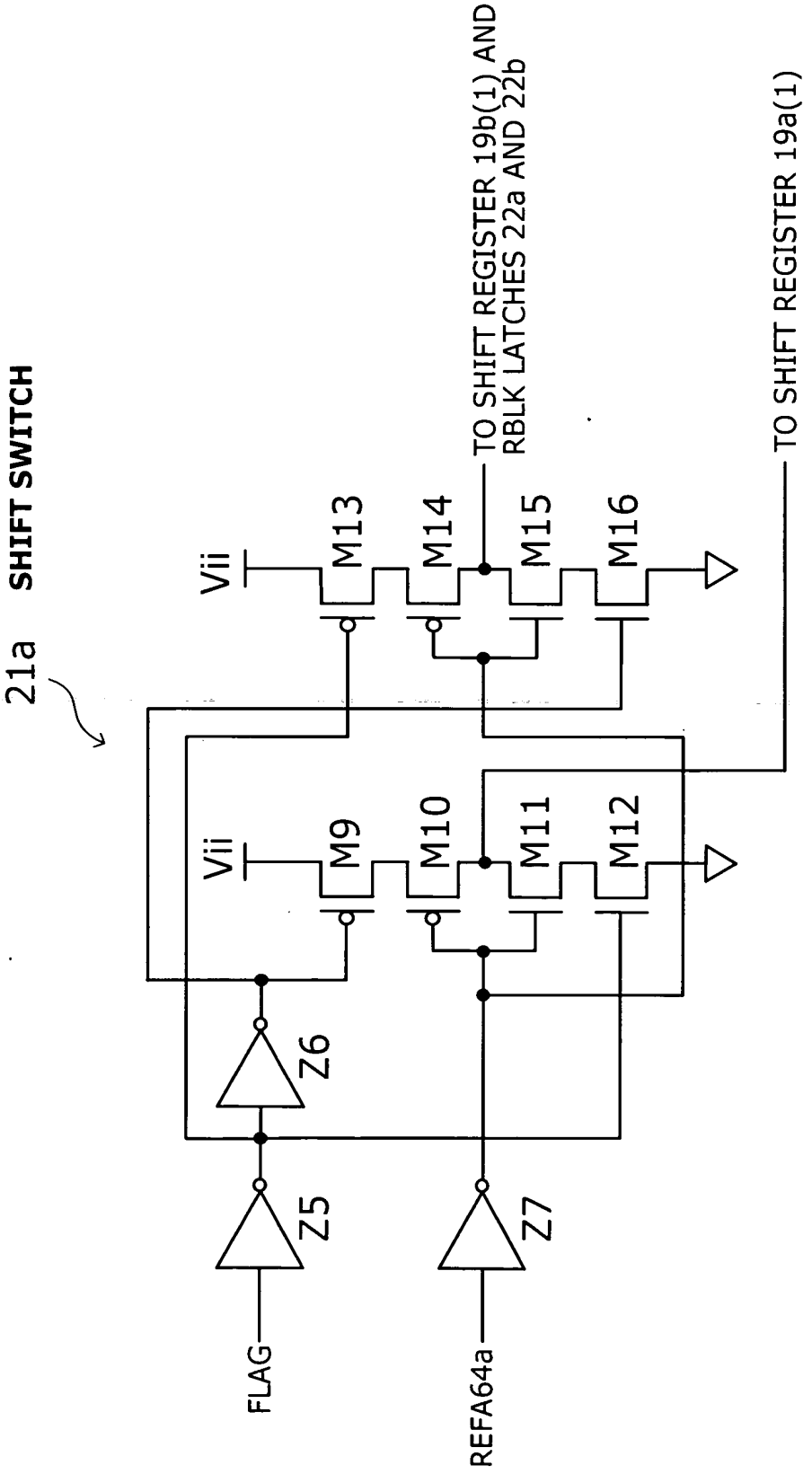

FIG. 5

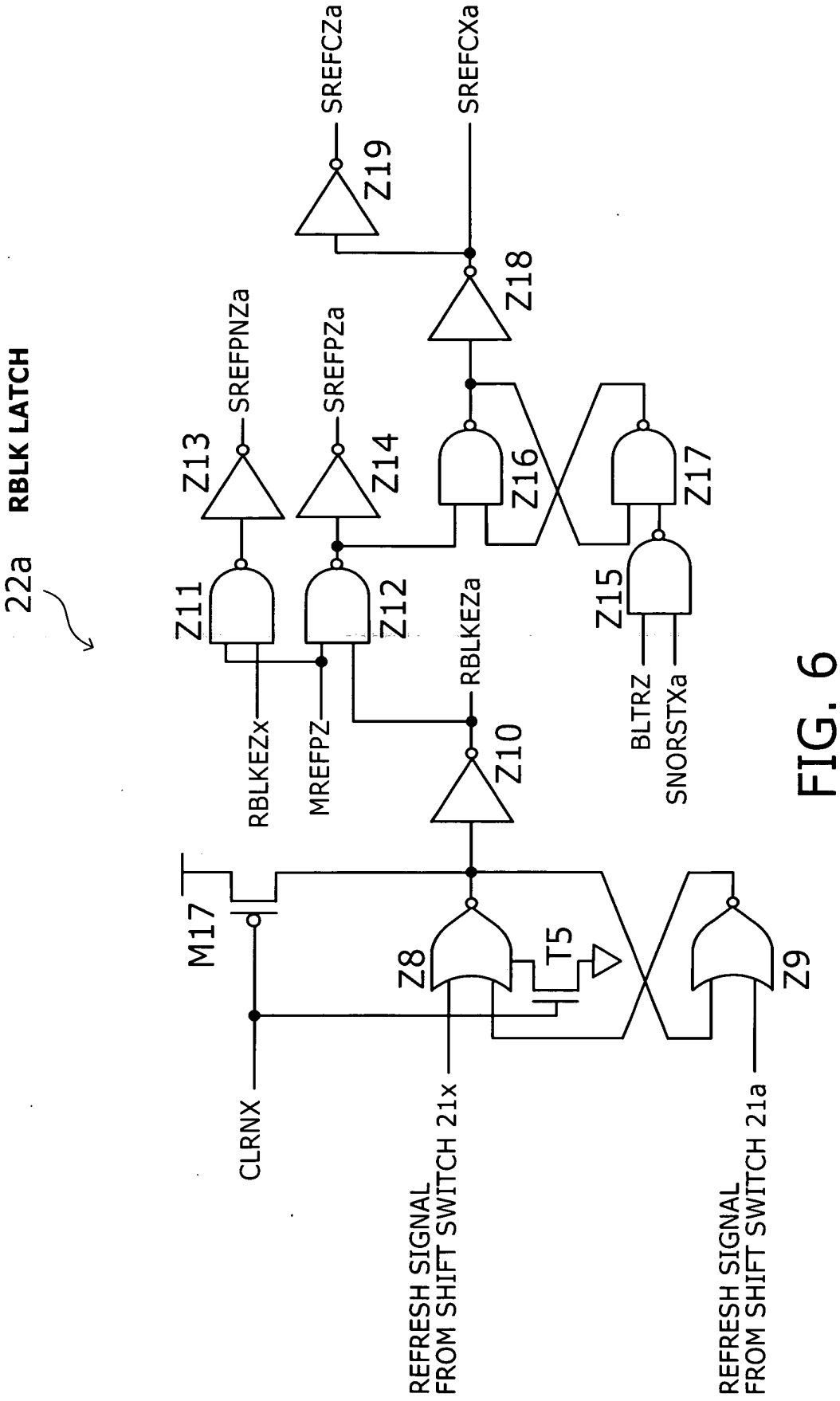
22a
RBLK LATCH
SREFCZa
SREFCXa
Z19
Z18
SREFPNZa
SREFPZa
Z13
Z14
Z16
Z17
Z11
Z12
Z15
RBLKEZa
RBLKEZx
MREFPZ
BLTRZ
SNORSTXa
Z10
M17
Z8
T5
Z9
CLRNX
REFRESH SIGNAL FROM SHIFT SWITCH 21x
REFRESH SIGNAL FROM SHIFT SWITCH 21a

FIG. 6

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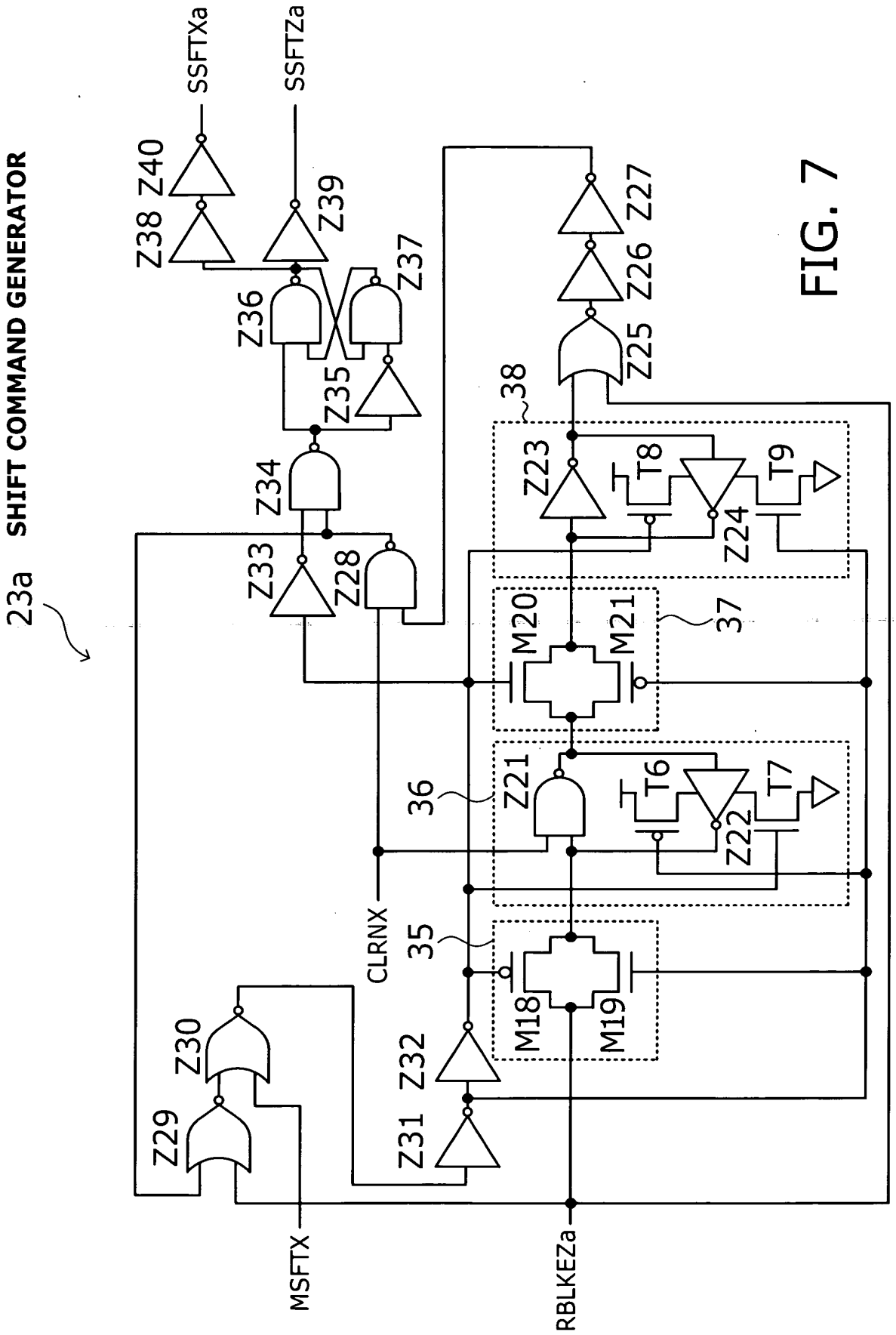

FIG. 7

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Docket No.: 108273-00007

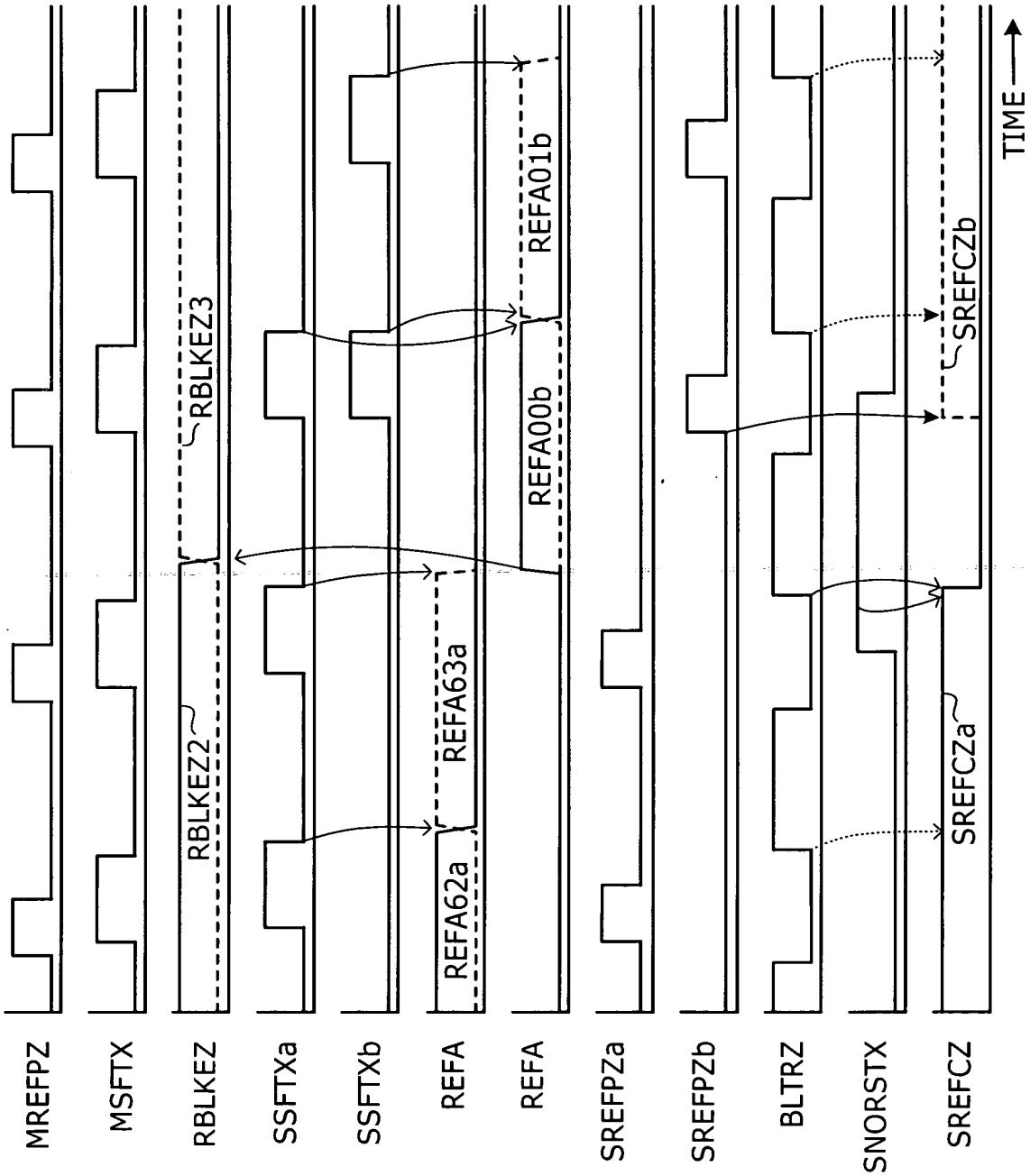

FIG. 8

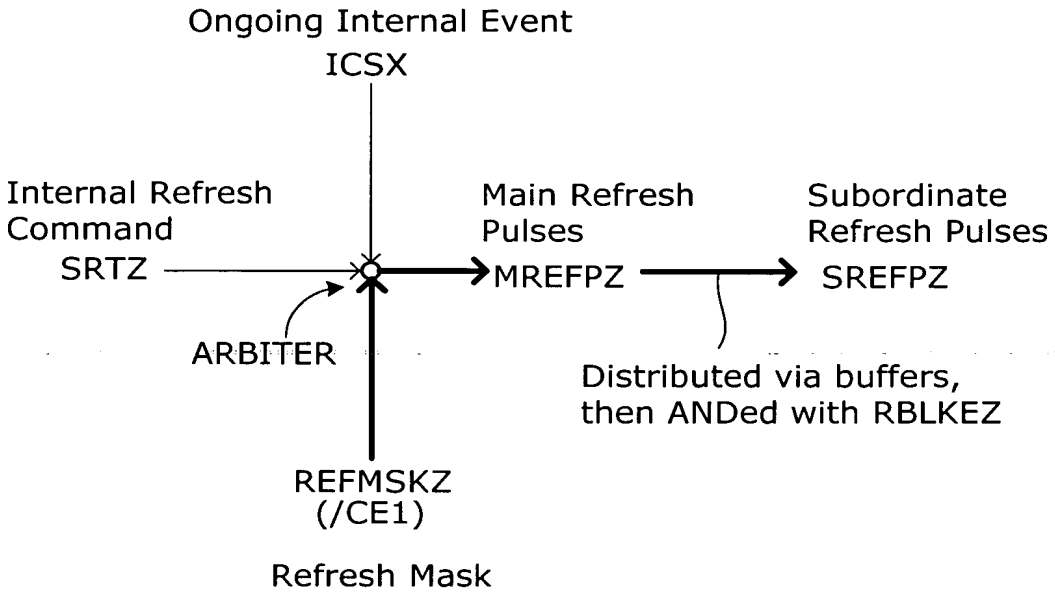
Ongoing Internal Event
ICSX
Internal Refresh Command
SRTZ
Main Refresh Pulses
MREFPZ
Subordinate Refresh Pulses
SREFPZ
ARBITER
Distributed via buffers, then ANDed with RBLKEZ
REFMSKZ
(/CE1)
Refresh Mask

FIG. 9

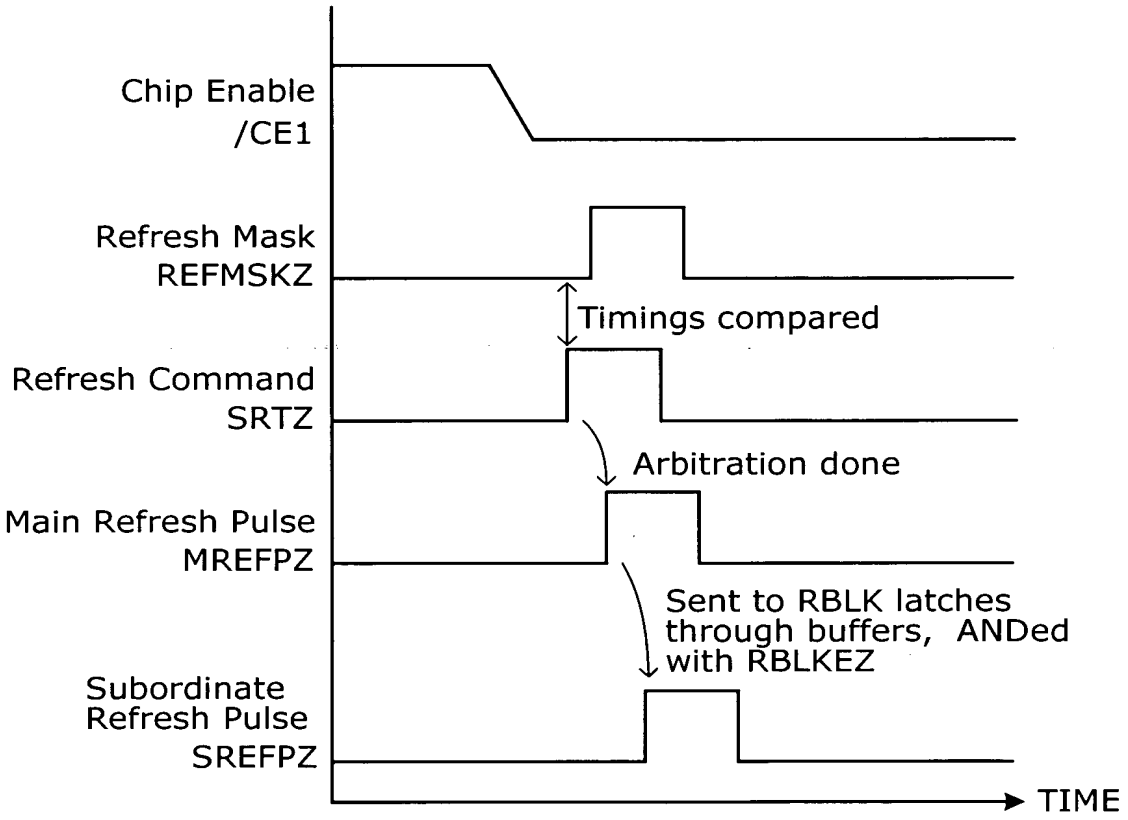
Chip Enable
/CE1
Refresh Mask
REFMSKZ
Timings compared
Refresh Command
SRTZ
Arbitration done
Main Refresh Pulse
MREFPZ
Sent to RBLK latches
through buffers, ANDed
with RBLKEZ
Subordinate
Refresh Pulse
SREFPZ
TIME

FIG. 10

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT REGISTER-BASED REFRESH ADDRESS GENERATION CIRCUIT
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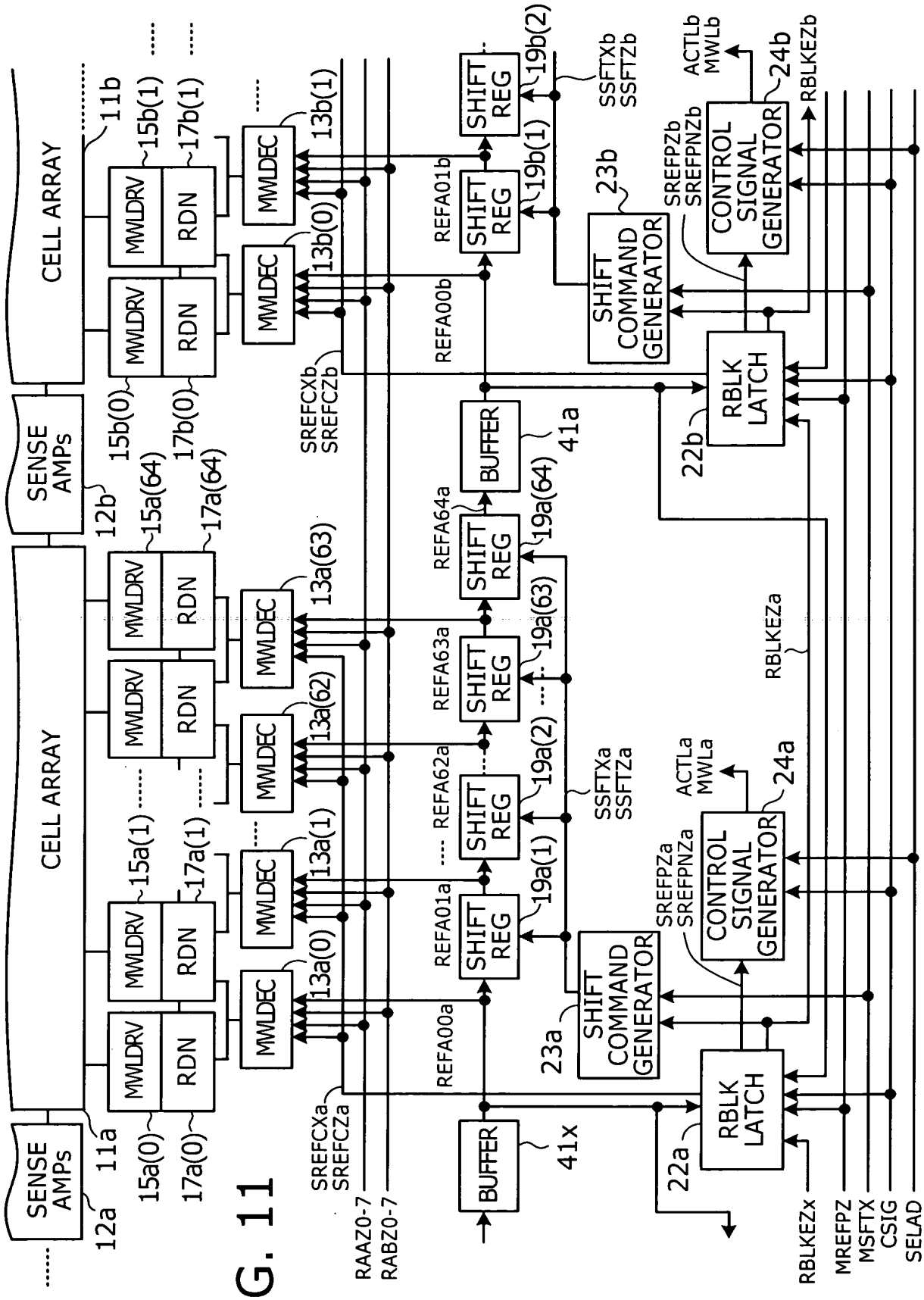

FIG. 11

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT REGISTER-BASED REFRESH ADDRESS GENERATION CIRCUIT
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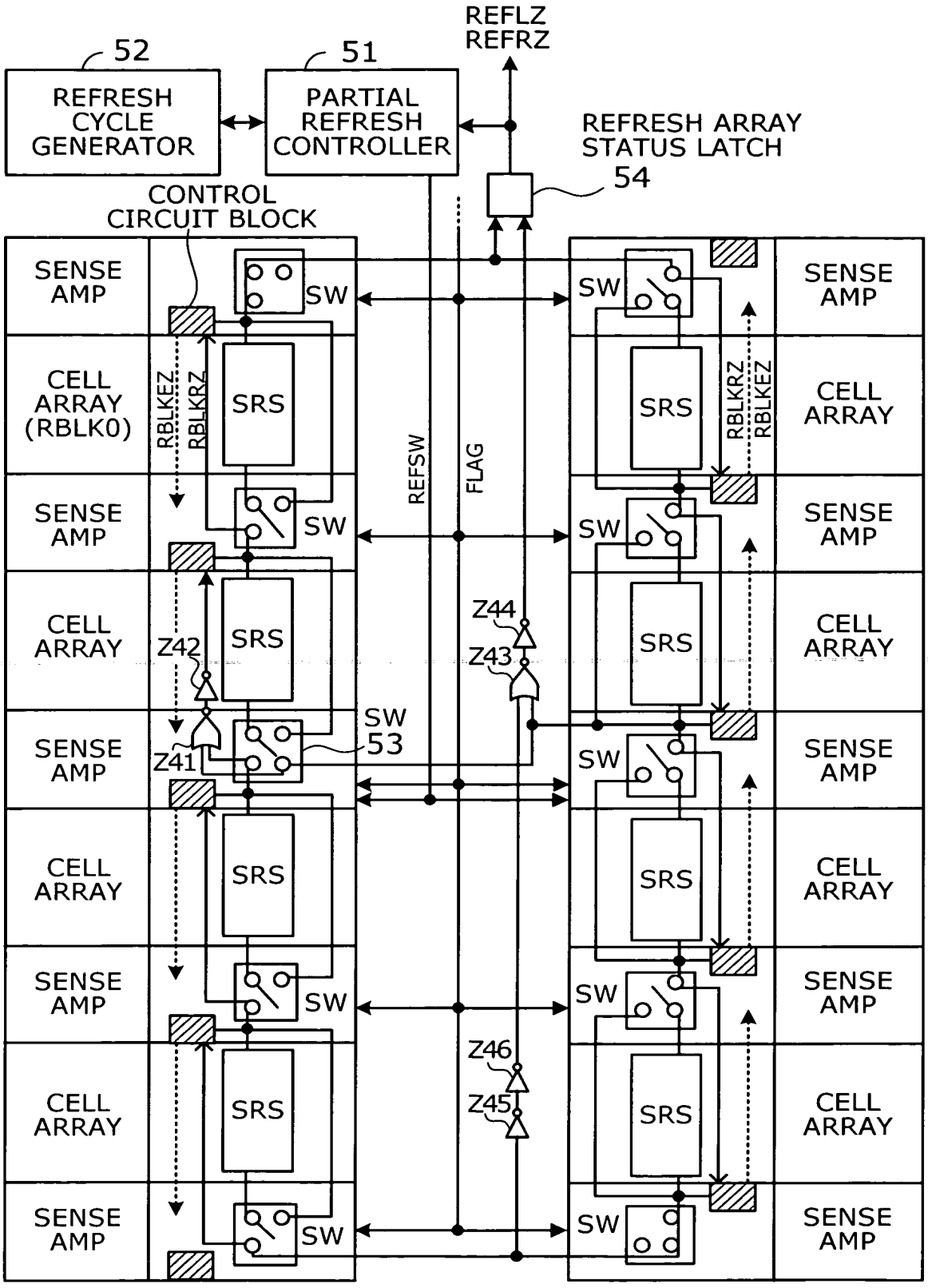

FIG. 12

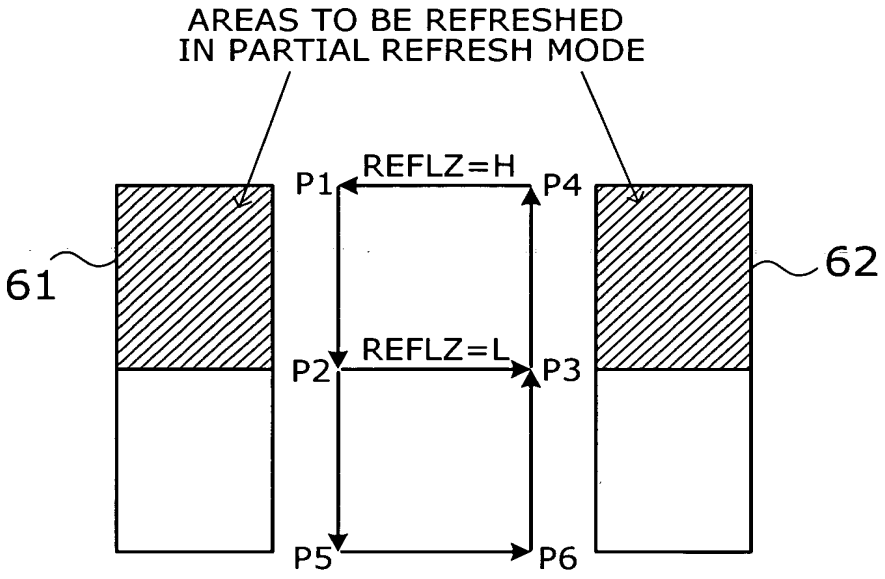
AREAS TO BE REFRESHED
IN PARTIAL REFRESH MODE
REFLZ=H
P1
P4
61
62
REFLZ=L
P2
P3
P5
P6

FIG. 13

	CONDITION	AREA SIZE	INTERVAL
NORMAL	CE2=H	x1	x1
ENTRY TO PARTIAL REFRESH MODE	CE2=L	x1	x1
PARTIAL REFRESH	REFLZ=H (1st)	x1/2	x2
EXIT FROM PARTIAL REFRESH MODE	CE2=H	x1/2	x1/2
EXIT (continued)	REFLZ=H (1st)	x1	x1/2
RETURN TO NORMAL	REFLZ=H (2nd)	x1	x1

FIG. 14

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT REGISTER-BASED REFRESH ADDRESS GENERATION CIRCUIT
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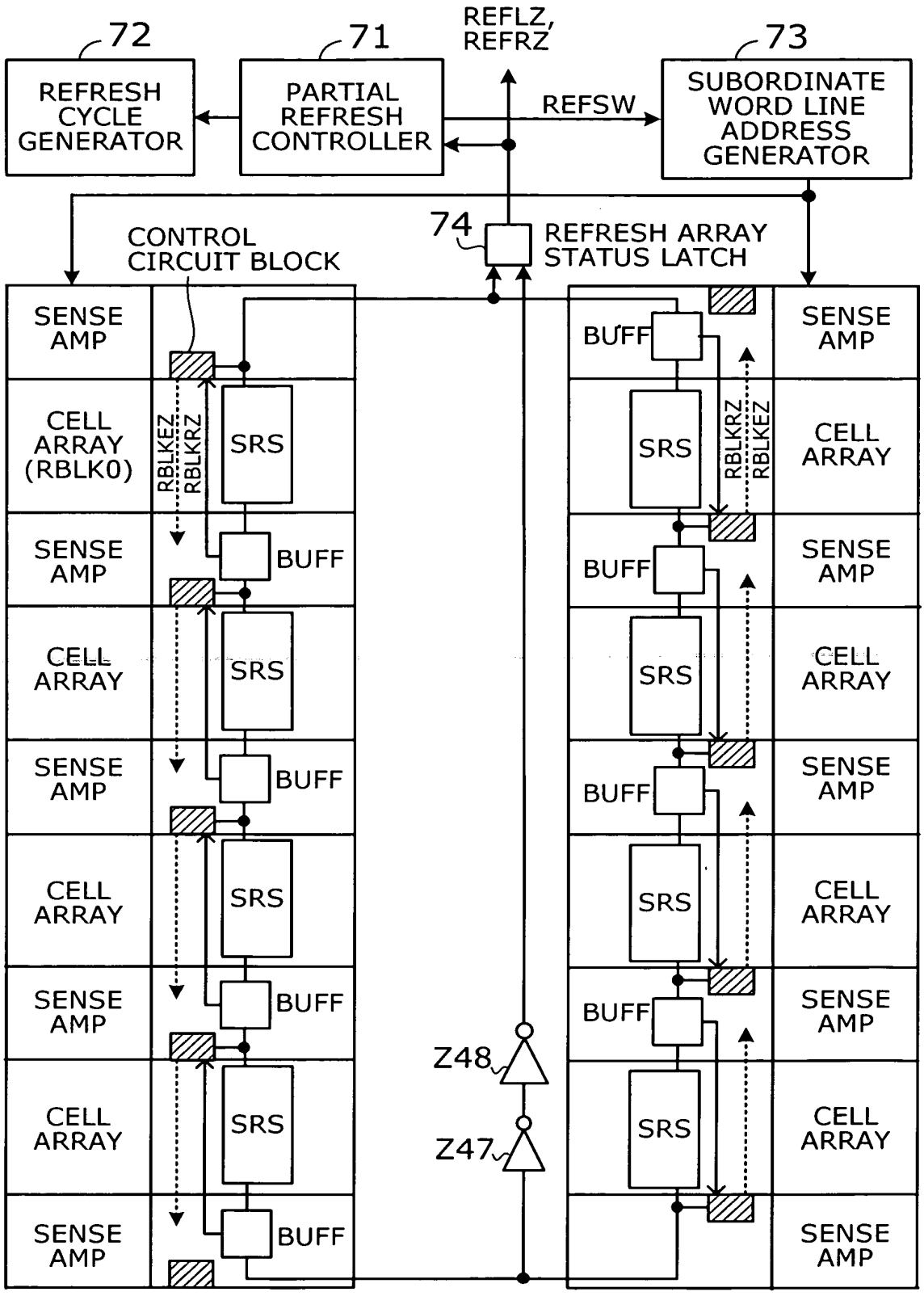

FIG. 15

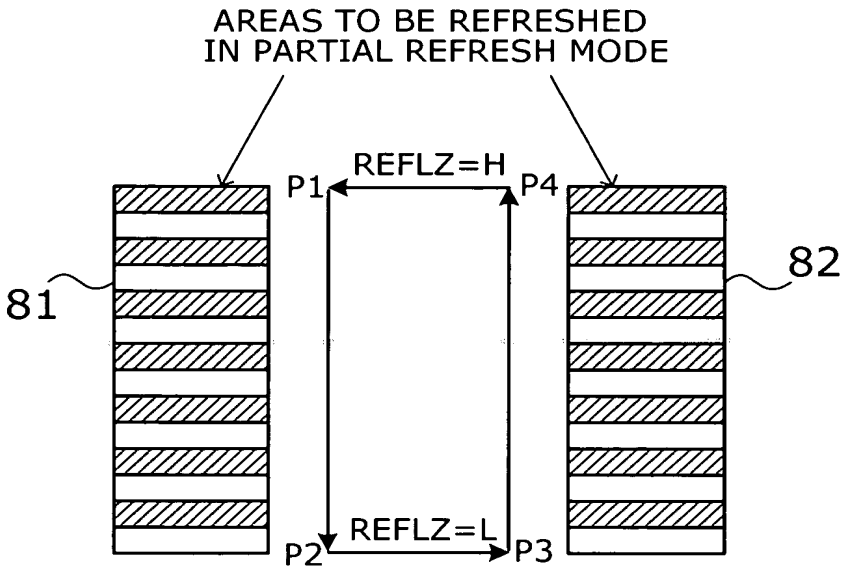
AREAS TO BE REFRESHED
IN PARTIAL REFRESH MODE
REFLZ=H
P1
P4
81
82
REFLZ=L
P2
P3

FIG. 16

	CONDITION	AREA SIZE	INTERVAL
NORMAL	CE2=H	x1	x1
ENTRY TO PARTIAL REFRESH MODE	CE2=L	x1	x1
PARTIAL REFRESH	REFLZ=H (1st)	x1/2	x2
EXIT FROM PARTIAL REFRESH MODE (RETURN TO NORMAL)	CE2=H	x1	x1

FIG. 17A

	CONDITION	AREA SIZE	INTERVAL
NORMAL	CE2=H	x1	x1
ENTRY TO PARTIAL REFRESH MODE	CE2=L	x1/2	x1
EXIT FROM PARTIAL REFRESH MODE (RETURN TO NORMAL)	CE2=H	x1	x1

FIG. 17B